PVP 19

Code: 19EC3401, 19EE3402

II B.Tech - II Semester – Regular Examinations – AUGUST 2021

DIGITAL LOGIC DESIGN

(Common to ECE, EEE)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 5 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each question carries 12 marks.
4. All parts of Question paper must be answered in one place

PART – A

1. a) Convert the given Decimal number to Octal.
$(15)_{10}$ = ($)_8$
b) Simplify the Boolean function $F(x, y) = \sum m(0,2)$
c) Define Universal gate.
d) Convert SR flip flop to JK flip flop.
e) Define counter.

PART – B

UNIT – I

2. a) Explain the Procedure for finding 2's complement subtraction of any two binary numbers. 6 M
b) Discuss the error detection and correction codes. 6 M

OR

3. a) Simply the following Boolean function into minimum literals 6 M
   i) (X+XY) ii) XY+X'Z+YZ
   b) Perform the 10's complement of the following decimal numbers. 6 M
   i)123456 ii) 676767

UNIT – II

4. a) Reduce the following function using K-map 6 M
   $F(A,B,C,D) = \Sigma\, m(0,1,2,4,5,8,9,12,13)$
   b) Draw the logic diagram using only 2- input NAND gates for XOR gate. 6 M

OR

5. a) Minimize the following function using K-map 6 M
   $F(w,x,y,z) = \Sigma\, m(0,1,4,5,8,9) + d(3,2,10,11)$
   b) Draw the logic diagram using only 2- input NOR gates for F= (AB)' 6 M

UNIT-III

6. a) Explain the operation of 4x1 multiplexer 6 M

   b) Design half adder using 2x4 Decoder. 6 M

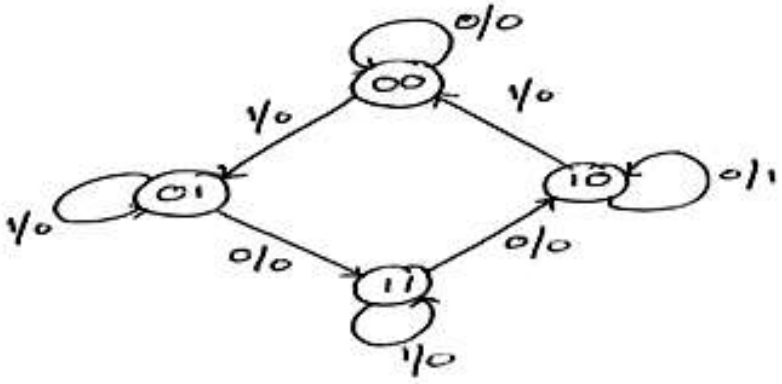
OR

7. a) Implement the following Boolean function using multiplexer. $F = S_1' S_0' A + S_1 S_0 B$ 6 M
   b) Discuss about Read and Write operation in Random access memory. 6 M

UNIT – IV

8. a) Explain the operation of D flip flop with truth table. 6 M

   b) Design a synchronous sequential circuit using T Flip-Flops for the given state diagram. 6 M



OR

9. a) Explain the operation of JK flip flop with truth table. 6 M

   b) Write down the design procedure for synchronous sequential circuits. 6 M

UNIT – V

10. a) Design a 4 bit binary synchronous counter with D Flip-Flop. 6 M

    b) Explain the operation of CMOS transmission gate. 6 M

OR

11. a) Discuss the following terms in relation to integrated circuits. 4 M

        i) Fan out ii) Power dissipation.

    b) Design and explain the 2-input CMOS NOR gate. 8 M